Abstract

A scan test circuitry design imbedded on an SoC having the scan architecture of a VLCT platform is disclosed herein. This BIST circuitry design that is not limited in the number of scan test ports supported includes at least one scan chain group having a corresponding clock domain that couples to receive test stimulus data. Each scan chain group has a corresponding test mode signal to shift the test stimulus data at a shift clock rate derived from its corresponding clock domain. A controlling demultiplexer connects to each multiplexer unit within each scan chain group to provide control signals for shifting in the test stimulus. A clock control mechanism provides a control signal for each scan chain to shift test stimulus and capture resultant data. Furthermore, when a simultaneous test mode signal is enabled, the clock control mechanism couples to each scan chain to enable simultaneous capture of each scan chain group.